In The Claims

1. (Canceled)

2. (Previously Presented) The node of Claim 28, wherein a Host Channel Adapter (HCA) couples the first processors to the first switch.

3. (Previously Presented) The node of Claim 2, wherein a peripheral component interconnect (PCI) bridge further couples the first processors to the first switch.

4. (Previously Presented) The node of Claim 28, wherein a link supporting processor-to-processor communication communicably couples the first processors directly to each other.

5. (Previously Presented) The node of Claim 28, wherein a Northbridge communicably couples the first processors to the first switch.

6. (**Currently Amended**) The node of Claim 28, wherein the first switch is ~~operable~~ **configured** to communicate input/output (I/O) messages at a bandwidth that is approximately equal to a processing speed of the first processors.

7. (Previously Presented) The node of Claim 28, wherein the integrated switch comprises twenty-four ports and enables a toroidal topology comprising four dimensions.

8. (**Currently Amended**) The node of Claim 28, wherein the integrated switch is ~~operable~~ **configured** to communicate a first message from a first one of the first processors and a second message from a second one of the first processors in parallel.

9. **(Currently Amended)** A system comprising a plurality of interconnected nodes, each node comprising:

a first motherboard;

at least two first processors integrated onto the first motherboard and ~~operable~~ **configured** to communicate with each other via a direct link between them; and

a first switch integrated onto the first motherboard, the first processors communicably coupled to the first switch, the first switch ~~operable~~ **configured** to communicably couple the first processors to at least six second motherboards that each comprise at least two second processors integrated onto the second motherboard and a second switch integrated onto the second motherboard ~~operable~~ **configured** to communicably couple the second processors to the first motherboard and at least five third motherboards that each comprise at least two third processors integrated onto the third motherboard and a third switch integrated onto the third motherboard;

the first processors ~~operable~~ **configured** to communicate with particular second processors on a particular second motherboard via the first switch and the second switch on the particular second motherboard;

the first processors ~~operable~~ **configured** to communicate with particular third processors on a particular third motherboard via the first switch, a particular second switch on a particular second motherboard between the first motherboard and the particular third motherboard, and the third switch on the particular third motherboard without communicating via either second processor on the particular second motherboard.

10. (Previously Presented) The system of Claim 9, wherein a Host Channel Adapter (HCA) couples the first processors to the first switch.

11. (Previously Presented) The system of Claim 10, wherein a peripheral component interconnect (PCI) bridge further couples the first processors to the first switch.

12. (Previously Presented) The system of Claim 9, wherein, at each of one or more of the nodes, a link supporting processor-to-processor communication communicably couples the first processors directly to each other.

13. (Previously Presented) The system of Claim 9, wherein a Northbridge communicably couples the first processors to the first switch.

14. **(Currently Amended)** The system of Claim 9, wherein the first switch is ~~operable~~ **configured** to communicate input/output (I/O) messages at a bandwidth that is approximately equal to a processing speed of the first processors.

15. (Previously Presented) The system of Claim 9, wherein the first switch comprises twenty-four ports and enables a toroidal topology comprising four dimensions.

16. (Previously Presented) The system of Claim 9, wherein the plurality of nodes are arranged in a topology enabled by the first switch of each of the plurality of nodes.

17. (Previously Presented) The system of Claim 16, wherein the topology comprises a hypercube.

18. (Previously Presented) The system of Claim 16, wherein the topology comprises a folded topology.

19. (Previously Presented) The system of Claim 9, wherein a first node of the plurality of nodes is interconnected to a second node of the plurality of nodes along an X axis, a third node of the plurality of nodes along a Y axis that is perpendicular to the X axis, a fourth node of the plurality of nodes along a Z axis that is perpendicular to the X and Y axes, and a fifth node along a diagonal axis that is oblique to one or more of the X, Y, or Z axes.

20. **(Currently Amended)** The system of Claim 19, wherein the connection between the first node and the fifth node is ~~operable~~ **configured** to reduce message jumps among the plurality of nodes.

21. **(Currently Amended)** A method comprising:

integrating at least two first processors onto a first motherboard, the first processors being ~~operable~~ **configured** to communicate with each other via a direct link between them; and

integrating a first switch onto the first motherboard and coupling the first switch to the first processors, the first processors communicably coupled to the first switch, the first switch ~~operable~~ **configured** to communicably couple the first processors to at least six second motherboards that each comprise at least two second processors integrated onto the second motherboard and a second switch integrated onto the second motherboard ~~operable~~ **configured** to communicably couple the second processors to the first motherboard and at least five third motherboards that each comprise at least two third processors integrated onto the third motherboard and a third switch integrated onto the third motherboard, the first processors ~~operable~~ **configured** to communicate with particular second processors on a particular second motherboard via the first switch and the second switch on the particular second motherboard, the first processors ~~operable~~ **configured** to communicate with particular third processors on a particular third motherboard via the first switch, a particular second switch on a particular second motherboard between the first motherboard and the particular third motherboard, and the third switch on the particular third motherboard without communicating via either second processor on the particular second motherboard.

22. (Previously Presented) The method of Claim 21, wherein coupling the first switch to the first processors comprises coupling each one of the first processors to the first switch through a Host Channel Adapter (HCA).

23. (Previously Presented) The method of Claim 22, wherein coupling the first switch to the first processors comprises coupling each one of the first processors to the first switch through a peripheral component interconnect (PCI) bridge.

24. (Previously Presented) The method of Claim 21, further comprising coupling at least two of the first processors directly to each other via a link supporting processor-to-processor communication.

25. (Previously Presented) The method of Claim 21, wherein coupling the first processors to the first switch comprises coupling each one of the first processors to the first switch through a Northbridge.

26. **(Currently Amended)** The method of Claim 21, wherein the first switch is ~~operable~~ **configured** to communicate input/output (I/O) messages at a bandwidth that is approximately equal to a processing speed of the first processors.

27. (Previously Presented) The method of Claim 21, wherein the integrated switch comprises twenty-four ports and enables a toroidal topology comprising four dimensions.

28. **(Currently Amended)** A node comprising:

a first motherboard;

at least two first processors integrated onto the first motherboard and ~~operable~~ **configured** to communicate with each other via a direct link between them; and

a first switch integrated onto the first motherboard, the first processors communicably coupled to the first switch, the first switch ~~operable~~ **configured** to communicably couple the first processors to at least six second motherboards that each comprise at least two second processors integrated onto the second motherboard and a second switch integrated onto the second motherboard ~~operable~~ **configured** to communicably couple the second processors to the first motherboard and at least five third motherboards that each comprise at least two third processors integrated onto the third motherboard and a third switch integrated onto the third motherboard;

the first processors ~~operable~~ **configured** to communicate with particular second processors on a particular second motherboard via the first switch and the second switch on the particular second motherboard;

the first processors ~~operable~~ **configured** to communicate with particular third processors on a particular third motherboard via the first switch, a particular second switch on a particular second motherboard between the first motherboard and the particular third motherboard, and the third switch on the particular third motherboard without communicating via either second processor on the particular second motherboard.

29. (Previously Presented) The node of Claim 28, further comprising an input port and an output port.

30. (Previously Presented) The node of Claim 5, comprising at least two Northbridges, each Northbridge communicably coupling one of the first processors to the first switch.

31. (Previously Presented) The system of Claim 13, each node comprising at least two Northbridges, each Northbridge communicably coupling one of the first processors to the first switch.

32. (Previously Presented) The method of Claim 25, wherein the motherboard comprises at least two Northbridges, each Northbridge communicably coupling one of the first processors to the first switch.

33. **(Currently Amended)** The system of Claim 9, wherein a first node of the plurality of nodes is interconnected to a second node, a third node, a fourth node, and a fifth node, the first node being the same as the second, third, fourth, and fifth nodes, the first node being ~~operable~~ **configured** to communicate with each of the second, third, fourth, and fifth nodes via the interconnections.